

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue of

U.S. Patent No. 5,526,313

Issued: June 11, 1996

For: LARGE SCALE INTEGRATED CIRCUIT WITH SENSE AMPLIFIER
CIRCUITS FOR LOW VOLTAGE OPERATION

DECLARATION, POWER OF ATTORNEY, AND PETITION

Assistant Commissioner of Patents
Washington, D.C. 20231
Sir:

Your petitioners, Jun Etoh, Kiyoo Itoh, Yoshiki Kawajiri, Yoshinobu Nakagome, Eiji Kume and Hitoshi Tanaka, citizens and residents of Japan, whose respective post office address is c/o Hitachi, Ltd. of Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, JAPAN, and/or Hitachi ULSI Systems Co., Ltd. of Tokyo, Japan, pray that they may be allowed to surrender and hereby offer to surrender the Letters Patent for an improvement in LARGE SCALE INTEGRATED CIRCUIT WITH SENSE AMPLIFIER CIRCUITS FOR LOW VOLTAGE OPERATION, U.S. Patent No. 5,526,313, granted to them on June 11, 1996. Hitachi, Ltd. and Hitachi ULSI Systems Co., Ltd., assignees of record, and of Tokyo, Japan, hereby offer to surrender said Letters Patent and assent to this accompanying reissue application as dual owners, by assignment, recorded in the United States Patent and Trademark Office. The undersigned petition that a Letters Patent be reissued to the said Hitachi, Ltd. and Hitachi ULSI Systems Co., Ltd., for the same invention upon the following amended specification, including claims.

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Jun Etoh, Kiyoo Itoh, Yoshiki Kawajiri, Yoshinobu Nakagome, Eiji Kume and Hitoshi Tanaka the above-named petitioners, verily believe themselves to be the original and first inventors of the invention described and claimed in U.S. Letters Patent No. 5,526,313 and in the foregoing reissue specification and for which improvement they solicit a reissue patent; that they do not know and do not believe that said improvement was ever known or used before this invention thereof; hereby state that they have reviewed and understand the contents of the above-identified specification, including the claims upon reissue; acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37 Code of Federal Regulations Section 1.56(a); hereby request that the patent formal drawings be transferred to this application. They hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with any divisional, continuation, continuation-in-part, reissue or reexamination application, with full power of appointment and substitution of associate attorneys and agents, and to receive all patents which may issue thereon;

John R. Mattingly, Registration No. 30,293
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The undersigned believe that U.S. Patent No. 5,526,313, is through error, without any deceptive intention, wholly or partly inoperative or invalid, by reason of a defective specification or drawing, or by reason of the patentee claiming more or less than the patentee had a right to claim in the patent. More specifically:

ERROR

The patentees had a right to claim all aspects of the invention. There is an error in that the patentees claimed less than they had a right to claim in the patent. Specifically, the patentees had a right to claim the embodiments of the invention shown in Figs. 20A-36C, which embodiments are supported by the specification beginning at page 25, line 37 and extending to page 39, line 61.

To correct the error through the present reissue application, applicants have submitted new claims 13-52, which are supported by the original disclosure and drawings of the patent. With respect to the new claims, claim 13 and 42 are the independent claims.

Claim 13 is supported by Fig. 20A and the specification at page 25, line 51 through page 26, line 50, for example. In particular, claim 13 refers to a first bias voltage, which has antecedent support in the specification as v_p , and a second bias voltage, which has antecedent basis in the specification as v_n .

Further claim 13 is supported by the description of Fig. 20A and the Description of the Preferred Embodiments, in general, for example page 4, lines 42-51, in which it is stated that the invention is directed to an LSI wherein the individual devices constituting the LSI chip may be "bipolar transistors, metal-insulator-semiconductor (MIS) transistors generally, metal-oxide semiconductor (MOSFET), [a] combination of these devices, or devices or material other than Si e.g. GaAs"; and still further at page 25, lines 45-50, which states, with reference to Figs. 20A, etc.:

"Although in the following example, complementary MOS-FETs are used, the other devices e.g. bipolar transistors or junction transistors, combination thereof with MOS-FET and devices made of semiconductor material (e.g. GaAs) other than silicon may be used."

The concordance between the claims and the figures and specification of the application is set forth as follows.

Claims 13-16 are supported by Figs. 20A through 21A. With respect to claim 15, see page 26, lines 30-37. Claims 17-18 are supported by Fig. 30A; claim 19 is supported by Fig. 31A and 31B; and claims 20-22 by Fig. 32A. Claim 23 is

supported by Fig. 33; claim 26 by Fig. 20B; and claim 31 by Fig. 23A. The remainder of the claims dependent on claim 13 as a base claim are supported in general by the specification and drawings, as mentioned above.

The other new independent claim is claim 42. Claim 42 is supported by Fig. 30A and claims 46 and 47 are supported by Figs. 20B and 23A, respectively. The remainder of the claims dependent on claim 42 as a base claim are supported by the specification and drawings in general.

Thus, the new claims presented in this reissue application, claims 13-52, are supported by the drawings and corresponding specification and are directed to the same invention that is disclosed in the original patent, as required under 35 U.S.C. § 251.

PRIORITY CLAIM

It is requested that the reissue application and reissue patent resulting therefrom receive the benefit of foreign priority under 35 U.S.C. § 119, specifically the benefit of Japanese Patent Applications:

No. 63-148104 filed June 17, 1988

No. 63-222317 filed September 7, 1988

No. 1-29803 filed February 10, 1989; and

No. 1-66175 filed March 20, 1989

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each filed in Japan. The certified priority documents were filed in the application resulting in U.S. Patent 5,526,313 and no additional certified copies are necessary in this reissue application.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

September 23, 1998
Date

Jun Etoh
Jun Etoh

October 6, 1998
Date

Kiyoo Itoh
Kiyoo Itoh

October 2, 1998
Date

Yoshiki Kawajiri
Yoshiki Kawajiri

September 21, 1998
Date

Yoshinobu Nakagome
Yoshinobu Nakagome

September 28, 1998
Date

Eiji Kume
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September 21, 1998
Date

Hitoshi Tanaka
Hitoshi Tanaka

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent
Application of: J. ETOH et al
Serial No. 09/095,101
Filed: June 10, 1998
Reissue of: U.S. Patent No. 5,526,313
Issued: June 11, 1996
For: LARGE SCALE INTEGRATED CIRCUIT
WITH SENSE AMPLIFIER CIRCUITS
FOR LOW VOLTAGE OPERATION

SUPPLEMENTAL RIGHT OF ASSIGNEE TO PROSECUTE REISSUE
APPLICATION - STATEMENT UNDER 37 CFR 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The assignees of the entire right, title and interest in and to the invention which is the subject of the above-identified reissue application are Hitachi, Ltd. and Hitachi VLSI Systems Co., Ltd.

A chain of title from the inventors of the patent identified above to the current assignees as follows.

1. From the the inventors to Hitachi, Ltd. and Hitachi VLSI Engineering Corporation in an assignment dated June 8, 1989.

This document was recorded in the Patent and trademark Office at Reel 5096, Frame 677.

2. From Hitachi VLSI Engineering Corporation to Hitachi ULSI Systems Co., Ltd. by a Change of Name Document dated April 1, 1998, with translation, showing that Hitachi VLSI Engineering Corp. was merged into Hitachi ULSI Systems Co., Ltd. on April 1, 1998.

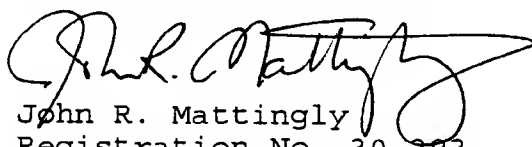
This document was recorded in the Patent and trademark Office at Reel 9605, Frame 0357.

The Assignment document and Change of Name document noted above establish documentary evidence of a chain of title from the inventors to the current assignees.

AUTHORIZATION TO SIGN STATEMENT

The undersigned attorney is authorized to sign this statement on behalf of the assignees.

Respectfully submitted,



John R. Mattingly
Registration No. 30,293
Attorney for Applicants

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Date: October 4, 2000